AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An apparatus comprising:

a data aligner to receive data, having a first data format ~~of~~ based on a system packet interface (SPI) protocol that has a first byte-length granularity of two bytes and a second data format ~~of~~ based on other than the SPI protocol that has a second byte-length granularity where the first and second byte-length granularities are different, from a data transmission link having a first data width and to align the data into predefined segments for interim storage, based on storage devices in which each storage device has a single read port and a single write port of a fixed byte length, the data aligner to multiplex each two-byte segment of the data in the first data format to remove interleaved command segments from the received data, prepend a fragment remaining from earlier received data when the fragment is present, and contiguously align remaining data segments to the fixed byte length boundary; and

a buffer, formed from the storage devices, to receive aligned data from the data aligner for interim storage and to reassemble data output onto a data path having a second data width that is wider than the first data width, the buffer to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the data path, based on the first and second byte-length granularity of the received data, and process fragmentation of data for alignment onto the data path by storing ~~the fragmentation~~ a fragment in a next selected storage device to prepend in a next byte length boundary, the buffer to use the storage devices in a cyclic manner based on the byte-length granularity of the received data, in which buffering of the received data of different byte-length granularity is achieved using storage devices having the single read port and the single write port.

2. (previously presented) The apparatus of claim 1, wherein the storage devices are arranged in arrays.

3. (currently amended) The apparatus of claim 2 further including a command control logic to separate ~~commands~~ the command segments from the data at an input to the data aligner and to process commands to align the data.

4. (previously presented) The apparatus of claim 3 further comprises a data re-aligner at the buffer output, wherein data entry may start in any one of the arrays and an orientation bit or bits is to be used to identify the starting array for re-alignment in the data re-aligner.

5. (original) The apparatus of claim 4 further including a meta-data unit to receive meta-data from the command control logic and to use the meta-data to realign the data in the data re-aligner.

6. (currently amended) The apparatus of claim 5 further comprising a data fragment collector to collect fragments ~~of data that do not fit into the predefined segment in one clock period and to use the fragment in a next clock period to fit into a next segment~~.

7. (previously presented) The apparatus of claim 1 wherein the first data format is based on SPI-4 protocol and the second data format is based on HyperTransport protocol.

8. (canceled)

9. (currently amended) An integrated circuit comprising:

an interface unit to receive incoming data from a higher frequency data transmission link having a first data width for use by the integrated circuit, the incoming data having a first data format ~~of~~ based on a system packet interface (SPI) protocol that has a first byte-length granularity of two bytes and a second data format ~~of~~ based on other than the API protocol that has a second byte-length granularity where the first and second byte-length granularities are different;

a command control unit to receive incoming data from the interface unit and to ~~separate commands~~ process commands from the received data ~~to process commands~~ to

align the data, the command control unit also to process interleaved command segments from the received data when the data is in the first data format;

a data aligner, coupled to the interface unit and the command control unit, to receive incoming data from the interface unit and to align the incoming data into a predefined segment for interim storage, based on storage devices in which each storage device has a single read port and a single write port of a fixed byte length, the data aligner to multiplex each two-byte segment of the data in the first data format after removal of the interleaved command segments from the received data, prepend a fragment remaining from earlier received data when the fragment is present, and contiguously align remaining data segments to the fixed byte length boundary; and

a reassembly buffer, formed from the storage devices, to receive aligned data from the data aligner for interim storage and to reassemble data output onto an internal data path having a second data width that is wider than the first data width, the reassembly buffer to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the internal data path, based on the first or second byte-length granularity of the received data, and process fragmentation of data for alignment onto the internal data path by storing ~~the fragmentation~~ a fragment in a next selected storage device to prepend in a next byte length boundary, the reassembly buffer to use the storage devices in a cyclic manner based on the byte-length granularity of the incoming data, in which buffering of the incoming data of different byte-length granularity is achieved using storage devices having the single read port and the single write port.

10. (previously presented) The integrated circuit of claim 9, wherein the storage devices are arranged in arrays.

11. (previously presented) The integrated circuit of claim 9, wherein the storage devices of the reassembly buffer are structured having multiple matrices arranged into arrays, in which a width of the individual matrix is determined by the second data width of the internal data path.

12. (original) The integrated circuit of claim 10 further comprises a data re-aligner at the reassembly buffer output, wherein an orientation bit or bits is generated at the data aligner and sent to the data re-aligner to be used to identify the starting array for re-alignment in the data re-aligner.

13. (original) The integrated circuit of claim 12 further including a meta-data unit to receive meta-data from the command control logic and to use the meta-data to realign the data in the data re-aligner.

14. (currently amended) The integrated circuit of claim 13 further comprising a data fragment collector to collect fragments ~~of data that do not fit into the predefined segment in one clock period and to use the fragment in a next clock period to fit into a next segment~~.

15. (previously presented) The integrated circuit of claim 9 wherein the first data format is based on SPI-4 protocol and the second data format is based on HyperTransport protocol.

16. (canceled)

17. (currently amended) A method comprising:

aligning data received from a data transmission link having a first data width into predefined segments for interim storage, wherein the received data has a first data format ~~of~~ based on a system packet interface (SPI) protocol that has a first byte-length granularity of two-bytes or a second data format ~~of~~ based on other than the SPI protocol that has a second byte-length granularity where the first and second byte-length granularities are different, wherein the aligning multiplexes each two-byte segment of the data in the first data format to remove interleaved command segments from the received data, prepends a fragment remaining from earlier received data when the fragment is present, and contiguously aligns remaining data segments to the fixed byte length boundary; and

buffering aligned data in a buffer for interim storage, in which the buffer is based on selected storage devices, in which each storage device has a single read port and a single write port of a fixed byte length, and the buffering to reassemble data output onto an internal data path of an integrated circuit having a second data width that is wider than the first data width, the buffering to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the internal data path, based on the first or second byte-length granularity of the received data, and process ~~fragmentation of data for alignment onto the internal data path~~ a fragment to be prepended onto a next byte length boundary, but the buffering is achieved through buffer arrays in a cyclic manner based on the byte-length granularity of the incoming data and in which the buffering of the incoming data of different byte-length granularity is achieved using storage devices having the single read port and the single write port.

18. (canceled)

19. (previously presented) The method of claim 17 wherein the buffering allows a data entry to start in any one of the arrays and an orientation bit or bits is used to identify the starting array for aligning and subsequent re-aligning at the output of the buffer.

20. (previously presented) The method of claim 19 wherein the first data format is based on SPI-4 protocol and the second data format is based on HyperTransport protocol.

21. (canceled)